CLAIMS

1. A frequency-voltage mechanism for power management, comprising:

a first PLL that generates a first source clock signal at a first frequency based on a bus clock signal;

a second PLL that generates a second source clock signal at a second frequency based on a first frequency control signal and said bus clock signal;

select logic that selects between said first and second source clock signals to provide a core clock signal based on a select signal;

clock control logic that detects power conditions via at least one power sense signal, that provides said first frequency control signal according to said power conditions, and that provides said select signal; and

voltage control logic, coupled to said clock control logic, that adjusts operating voltage commensurate with frequency of said core clock signal.

2. The frequency-voltage mechanism of claim 1, wherein said select logic switches said core clock signal via said select signal within one clock cycle of said bus clock signal.

3. The frequency-voltage mechanism of claim 1, wherein said second PLL generates a first frequency lock signal when said second source clock signal achieves a reduced frequency indicated by said first frequency control signal.

4. The frequency-voltage mechanism of claim 3, wherein said clock control logic controls said select signal to switch said core clock signal from said first PLL to said second PLL in response to said first frequency lock signal.

5. The frequency-voltage mechanism of claim 4, wherein said voltage control logic reduces said operating voltage after said core clock signal is switched.

6. The frequency-voltage mechanism of claim 4, wherein said voltage control logic increases said operating voltage in response to increase power conditions, and wherein said clock control logic switches to said first PLL after said operating voltage is increased.

7. The frequency-voltage mechanism of claim 6, further comprising:

said voltage control logic asserting a voltage step signal to adjust voltage; and

a power supply that adjusts said operating voltage based on said voltage step signal and that provides a voltage lock signal indicative thereof to said clock control logic.

8. The frequency-voltage mechanism of claim 1, wherein said first PLL generates said first clock source signal based on a second frequency control signal and that asserts a second lock signal indicative thereof, and wherein said clock control logic provides said second frequency control signal and receives said second lock signal.

9. The frequency-voltage mechanism of claim 1, wherein said clock control logic and said voltage control logic cooperate to increase said operating voltage prior to increasing frequency of said core clock signal and to decrease said operating voltage after decreasing frequency of said core clock signal.

10. A microprocessor, comprising:

a power condition sense interface receiving at least one power sense signal indicative of power conditions;

an operating voltage interface;

a first PLL that generates a first source signal at a frequency based on a bus clock signal and a first core ratio bus value and that provides a corresponding first lock signal;

a second PLL that generates a second source signal at a frequency based on said bus clock signal;

a clock controller, coupled to said power condition sense interface and said first and second PLLs, that provides a select signal for switching between said first and second PLLs, that provides said first core ratio bus value to control frequency of said first source signal and that receives said corresponding first lock signal;

select logic that selects between said first and second PLLs based on said select signal to provide a core clock signal; and

a voltage controller, coupled to said clock controller and said operating voltage interface, that adjusts operating voltage commensurate with frequency of said core clock signal.

11. The microprocessor of claim 10, wherein:

said second PLL generates said second source signal at a maximum power frequency level;

wherein said clock controller initially selects said second PLL, determines a reduced power level sufficient to meet said power conditions, provides said first core ratio bus value indicative of a reduced frequency of said core clock signal to achieve said reduced power level, and switches said select signal to select said first PLL in response to receiving said first lock signal;

wherein said first PLL ramps said first source signal to said reduced frequency and provides said first lock signal indicative thereof; and

wherein said voltage controller reduces operating voltage commensurate with said reduced frequency after said clock controller switches said core clock signal.

12. The microprocessor of claim 11, wherein:

said voltage controller detects an increased power level sufficient to meet said power conditions and increases operating voltage; and

wherein said clock controller switches said select signal to select said first PLL after operating voltage is increased.

13. The microprocessor of claim 10, further comprising:

said second PLL generating said second source signal at a frequency based on said bus clock signal and a second core ratio bus value and that provides a second lock signal indicative thereof; and

said clock controller providing said second core ratio bus value to control frequency of said second source signal and receiving said corresponding first lock signal.

14. The microprocessor of claim 13, wherein said clock controller and said voltage controller cooperate to decrease operating voltage after decreasing frequency of said core clock signal and to increase operating voltage before increasing frequency of said core clock signal.

15. A method of frequency-voltage control for microprocessor power management, comprising:

generating a first source clock at a first frequency based on a bus clock signal and a first ratio bus value;

generating a second source clock at a second frequency based on the bus clock signal and a second ratio bus value;

sensing power conditions;

switching core operating frequency between the first and second source clock signals based on sensed power conditions; and

selecting operating voltage commensurate with the core operating frequency.

16. The method of claim 15, further comprising:

initially selecting the first source clock signal;

providing the second ratio bus value based on reduced power conditions to indicate a reduced frequency;

ramping the second source clock signal to the reduced frequency in response to the second ratio bus value;

detecting a first lock indication when the second source clock signal achieves the reduced frequency;

switching to the second source clock signal when the lock indication is detected; and

reducing operating voltage commensurate with the reduced frequency after said switching.

17. The method of claim 16, wherein said switching to the second source clock signal comprises switching within one bus clock cycle.

18. The method of claim 16, further comprising:

sensing increased power conditions;

increasing operating voltage commensurate with the sensed power conditions; and

switching to the first source clock signal.

19. The method of claim 18, prior to said switching to the first source clock signal, further comprising:

determining an increased power level appropriate for the increased power conditions;

providing the first ratio bus value indicative of an increased frequency based on the increased power level;

ramping the first source clock signal to the increased frequency;

said increasing operating voltage comprising increasing operating voltage commensurate with the increased frequency; and

detecting a second lock indication when the first source clock signal achieves the increased frequency.

20. The method of claim 18, wherein said switching to the first source clock signal comprises switching within one bus clock cycle.